REMARKS

In the Office Action the Examiner noted that claims 1-6 and 9-31 are pending in the application. The Examiner allowed claims 1, 3, 5-6, 9-29, and 31, and rejected claims 2, 4, and 30. By this Amendment, claims 34-36 have been newly added. No new matter has been presented. Therefore, claims 1-6, 9-31, and 34-36 are pending in the application. The Examiner's rejections are traversed below, and reconsideration of all rejected claims is respectfully requested.

Claim Rejections Under 35 USC §102

In item 2 on pages 2-3 of the Office Action the Examiner rejected claims 2, 4, and 30 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,715,105, issued to Rearick (hereinafter referred to as "Rearick"). The Applicants respectfully traverse the Examiner's rejections of these claims.

Claim 2 of the present application recites a mask to convert an indeterminate value in outputs from said shift registers into a state value of "0" or "1" to mask said indeterminate value, and an output verifier to verify output results in which said indeterminate value is masked by said mask, said output results not containing said indeterminate value. The Applicants respectfully submit that at least these features are not disclosed in Rearick.

The Examiner stated that Rearick discloses a mask 105 to convert an indeterminate value in outputs from said shift registers into a state value of "0" or "1" to mask said indeterminate value. However, the Applicants respectfully submit that the mask 105 of Rearick does not convert the indeterminate values into a value at all, but merely precludes the indeterminate values from being sent to the signature analyzer 104. "Preferably, the input to the signature register 104 may be masked via a signature mask register 105 to allow various bits of the scan-out data SCAN_OUT to be ignored. The masking feature is useful for masking out unknown output data generated by uninitialized internal states, for example, present at the beginning of a test" (Column 6, Lines 11-17). Thus, the mask 105 apparently merely stops the indeterminate values from being supplied to the signature analyzer 104, rather than converting the indeterminate values to a "0" or "1" to mask the value. This is indirect contrast with claim 2, which recites a mask to convert an indeterminate value in outputs from said shift registers into a state value of "0" or "1" to mask said indeterminate value.

Also, the Examiner stated that Rearick discloses an output verifier to verify output results in which said indeterminate value is masked by said mask, said output results not containing said indeterminate value. The Examiner characterized the signature analyzer 104 as the output verifier to verify output results. However, the Applicants respectfully submit that the signature analyzer 104 performs no type of verification operation as recited in claim 2. Rather, the signature analyzer 104 merely receives the scan-out signals, minus the indeterminate values, from the mask 105, compresses the received signals, and generates a signature accordingly which will may be used in a data verification process (Column 7, Lines 6-15). Thus, the data to be later verified is output from the scan data out (SDO) port 128, "either directly (through one port of a multiplexer 138) or indirectly through a signature register 104 which compresses the scan-out data SCAN_OUT to generate a signature (through another port of the selectable multiplexer 138)" (Column 6, Lines 7-11). Therefore, the signature analyzer 104 performs no verification of output results in which said indeterminate value is masked, but merely generates a signature. Further, even if it were assumed, arguendo, that this signature generation could be a verification process, the signature is generated without signals that were indeterminate, because the mask causes them to be ignored (Column 6, Lines 11-14), rather than generating the signature with converted values in place of the indeterminate values. This is in direct contrast to the discussed features of claim 2.

Therefore, Rearick does not disclose or suggest at least the features of "a mask to convert an indeterminate value in outputs from said shift registers into a state value of "0" or "1" to mask said indeterminate value, and an output verifier to verify output results in which said indeterminate value is masked by said mask, said output results not containing said indeterminate value." Accordingly, Rearick does not disclose every element of the Applicants' claim 2. In order for a reference to anticipate a claim, the reference must teach each and every element of the claim (MPEP §2131). Therefore, since Rearick does not disclose the features recited in independent claim 2, as stated above, it is respectfully submitted that claim 2 patentably distinguishes over Rearick, and withdrawal of the §102(e) rejection is earnestly and respectfully solicited.

Claim 4 depends from claim 2 and includes all of the features of that claim plus additional features which are not disclosed or suggested by Rearick. Therefore, it is respectfully submitted that claim 4 also patentably distinguishes over Rearick.

Claim 30 of the present application also recites a mask to convert an indeterminate value in outputs from said shift registers into a state value of "0" or "1" to mask said

indeterminate value; and an output verifier to verify output results in which said indeterminate value is masked by said mask, said output results not containing said indeterminate value. Therefore, it is respectfully submitted that claim 30 also patentably distinguishes over Rearick.

New Claims 34-36

New claim 34 is directed to a testing apparatus, and new claim 36 is directed to an integrated circuit, each comprising a mask to specify a shift register to convert the indeterminate value into a state value of "0" or "1" to mask the indeterminate value, and an output verifier to verify the masked output results of the specified shift register, from which output results the indeterminate value is excluded. Further, new claim 35 depends from new claim 34.

Therefore, it is respectfully submitted that new claims 34-36 also patentably distinguish over Rearick.

Summary

In accordance with the foregoing, new claims 34-36 have been added. No new matter has been presented. Thus, claims 1-6, 9-31, and 34-36 are pending and under consideration.

There being no further outstanding objections or rejections, it is respectfully submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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